A3 has a wavelength of 532 nanometers, a pulse width of 16 nanoseconds, repetition rate of between 3 Hz and 10 Hz and an energy fluence of 0.1 to 0.3 Joules/cm^2.

Remarks

It is noted that the IDS that was submitted on May 13, 2002, was not considered by the Examiner in his action since they obviously crossed in the mail. It is respectfully requested that the Examiner review and consider the IDS in his next action.

The Drafting Examiner's comments and objections to Figures 1 and 6 have also been considered and it believed that the substitute drawings for those figures submitted herewith overcome those objections addressed each of them. The drawings are now believed to be in compliance with the rules with respect to drawings.

Claims 1-3, 6, 8-11 and 20-22 were rejected by the Examiner under 35 USC § 103(a) as being obvious over Ishida '605 in view of Talwar '476. since claims 1 and 11 are the independent claims in Applicants' application, the initial focus will be on those claims. Since the only difference between those claims is that in claim 1the dopant is **"introduced to"** the top surface of the amorphous silicon layer, whereas in claim 11 the dopant layer is **"formed on"** the top of the amorphous silicon layer, thus claim 1 will be used for the discussion here.

In abbreviated form, claim 1 calls the following method:

a) forming an insulation layer on said top surface of the silicon substrate;

b) forming an **amorphous silicon layer** on top of and in contact with said insulation layer;

c) introducing a dopant in a top surface layer of said **amorphous silicon layer**; and

d) irradiating said top surface layer of said **am rphous silicon layer** with a

radiation beam to heat said top surface layer and initiate **expl sive recrystallizati n of said amorphous silicon layer** thereby **transforming** said **amorphous silicon layer int a p lycrystalline silicon gate** and **distributing said d pant unif rmly throughout said polycrystalline gate.**

The above highlighted features of claim 1 it will be seen, as the discussion proceeds, are the features that distinguish claim 1 (and similarly claim 11) from Ishida.

Ishida, in column 3 of his patent states that he begins with a silicon wafer that is the substrate (50) and that "before forming the source/drain regions and doping the **polysilicon gate**, the circuit components are constructed within and on the substrate 50 in accordance with well known integrated circuit fabrication techniques." (lines 5-8) As shown in his Figure 2a, initially he has formed the isolation regions 52, gate oxide layer 54 with the **polysilicon gate** 56 thereon and sidewall spacers 57 surrounding the gate oxide and gate. (emphasis added)

Next the substrate 50 and the **polysilicon gate** 56 are doped to form unactivated source and drain regions 90 and 92, as well as an unactivated **polysilicon gate** 56. (lines 37-41) "After doping the **poly gate** 56, a laser anneal step is used to anneal the doped **poly gate** 56...thereby **driving** the impurities ions to a **desired depth** in the **poly**. Laser annealing is the preferred method for annealing because the laser energy **may be** set at a level that is high enough to melt the poly gate 56..." (lines 45-50) (emphasis added)

"Note that the impurity ions are preferably **not** driven down the entire depth of the **poly** because the **poly gate** 56 will be exposed to subsequent thermal processing during the formation of the source/drain regions and therefore the impurity ions will further diffuse. The laser anneal step, **does**, however, provide **a substantial am unt of poly diffusi n**..." (lines 52-58) (emphasis added)

"After the **poly gate** anneal is completed, a standard RTA is performed to activate the unactivated source and drain regions 90 and 92 **and perform additi nal impurity diffusi n in the p ly gate 56**...The RTA also causes the impurities to diffuse through the entire depth of the **poly**, thereby eliminating poly depletion." (lines 61-70) (emphasis added)

Summarizing, Applicants' claim 1 begins with an amorphous silicon layer that is doped and then irradiated to cause explosive recrystallization producing a polysilicon gate with the dopant uniformly distributed throughout.

Ishida begins with a polysilicon gate that is doped and then first annealed to drive the impurities ions to a **desired depth** in the **polysilicon**. (Ishida here notes that the laser **may be** set at a level that is high enough to melt the poly gate 56 **BUT NOT REQUIRED**.) he then requires a **second** process step, a standard RTA to activate the unactivated source and drain regions 90 and 92 **and perform additional impurity diffusion in the poly gate 56** to causes the impurities to diffuse through the entire depth of the **poly**.

The Examiner states in his comments with regard to Ishida:

> " Ishida teaches a polysilicon gate structure (56) overlying an insulation layer (54), which overlies a silicon substrate (50). Ishida also teaches doping the polysilicon gate structure (Figure 2b) and annealing the doped gate structure with a laser (Figure 2c) to promote **crystallization** and distribution of the dopant. (See column 3 lines 16-60 and Figures 2a-2c)" (emphasis add)

No where does Ishida state that his process promotes **crystallization** of the polysilicon gate structure, not in the section of the patent pointed out by the Examiner, or anywhere else in the patent. Ishida says he first drives the impurities ions to a

desired depth in the **p lysilicon,** and then second, in the RTA step, performs additional impurity diffusion in the poly gate. Additionally, Ishida n where states or suggests that amorphous silicon can be substituted for the polysilicon gate.

The definitions of "polysilicon" and "amorphous silicon" are as follows:

"INTERNATIONAL SEMATECH OFFICIAL DICTIONARY, REV 5.0

(http://www.sematech.org/public/publications/dict/)

This dictionary defines terms that are used in the semiconductor manufacturing industry. It is intended to foster a common language within the International SEMATECH community and within the industry. Some terms are specific to International SEMATECH, but others are collected from industry standards (see Doc Info).

polycrystalline silicon (poly)

n

1 : a nonporous form of silicon made up of randomly oriented crystallites or domains, including glassy or amorphous silicon layers. [ASTM F399-88] 2 : silicon formed by chemical vapor deposition from a silicon source gas or other methods and having a structure that contains large-angle grain boundaries, twin boundaries, or both. [SEMI M16-89] Also called *poly* and *polysilicon.* Contrast amorphous silicon and single crystal.

amorphous silicon

n

silicon with no discernible crystalline structure. [SEMATECH] Contrast polycrystalline silicon."

From these definitions it can be seen that polysilicon is a crystalline form of silicon whereas amorphous silicon has no discernible crystalline structure. Thus, since polysilicon is already in crystalline form Ishida would not even have considered using the technique of explosive recrystallization to disperse the dopant. That technique may not have even worked when starting with a crystalline form of silicon. Additionally, Ishida only says that one **may** heat the poly layer to melting, however, he suggests that the poly layer only be heated to drive the dopant to a desired level. If the poly layer is melted then one can not control the depth to which the dopant is driven.

Therefore, since polysilicon is already crystalline and Ishida teaches away from melting the polysilicon layer, it can be said that crystallization of the polysilicon layer did not cross Ishida's mind.

The Examiner then adds Talwar '476 to introduce an amorphous silicon layer in place of the polysilicon layer of Ishida. However, Ishida's method first controls the depth to which the dopant is driven in the first anneal step and completes the process in his second RTA step, both without recrystallizing the gate material. If the amorphous layer of Talwar '476 is not recrystallized then the gate will not function as desired.

Thus, the combination of Ishida and Talwar '476 can not be said to make the process of Applicants' claims 1 and 11 obvious from that combination of references. Further, since claims 2-3, 6, 8-10 and 20-22 are each dependent from claim 1 or 11, the same holds true for those claims as for claims 1 and 11. Therefore, none of claims 1-3, 6, 8-11 and 20-22 can be said to be obvious from Ishida in view of Talwar '476.

Claims 4, 5, 16 and 17 were rejected by the Examiner under 35 USC § 103(a) as being obvious over Ishida '605 in view of Talwar '488. Claims 4 and 5 are dependent from independent claim 1, and claims 16 and 17 are dependent from independent claim 11, thus the same argument with respect to Ishida and claims 1 and 11 above applies. The addition of Talwar'488 does not add the missing disclosure of Ishida, therefore claims 4, 5, 16 and 17 are distinguishable from Ishida and Talwar '488.

Claims 7, 12-14 and 19 were rejected by the Examiner under 35 USC § 103(a) as being obvious over Ishida '605. Claim 7 is dependent from claim 1, and claims 12-14 and 19 are dependent from claim 11. Therefore, the same argument above with respect to Ishida and claims 1 and 11 is applicable here as well. Thus, claims 7, 12-14 and 19 are patentably distinguishable from Ishida.

Claim 23 was rejected by the Examiner under 35 USC § 103(a) as being obvious over Ishida in view of Zhang. Claim 23 is dependent from independent claim 11, thus the same argument with respect to Ishida and claim 11 above applies to claim 23. The addition of Zhang does not add the missing disclosure of Ishida, therefore claim 23 is distinguishable from Ishida and Zhang.

All claims having been shown to be non-obvious from Ishida, either alone or in combination with one of the other cited references, are therefore each patentably distinguishable from the cited references and thus in condition for allowance.

It is respectfully requested that the Examiner withdraw his rejections of the various claims and send the application to allowance.

Favorable action is respectfully requested.

Respectfully submitted,
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